THE UNIVERSITY of ADELAIDE

Summer Research Scholarships

School of Electrical and Electronic Engineering

Project Titles 2017/18

Algorithms for Measuring Sleep Health
Description: Sleep performs important restorative functions for brain and body. Since we spent about 1/3rd of our lives asleep, sleep disturbance can seriously affect emotional wellbeing, cognitive performance and cardiovascular health. It is therefore important to monitor sleep if issues are suspected. Multichannel sleep recordings, performed at home or hospital, acquire a number of physiological signals throughout the night, creating large volumes of biological data. Automated algorithms are required to process these signals and deliver diagnostic information to aid clinical decision making. In this project, we will analyze nasal airflow signals obtained during a large, international randomized trial involving >2,000 patients to create a robust algorithm for detecting airflow limitations. This project will develop students' skills in biomedical signal processing using Matlab and background knowledge in sleep physiology.
Supervisors: A/Prof Mathias Baumert and Dr Dominik Linz

Developing Artificially Intelligent Control for a Robot Soccer Table
Description: This project provides an opportunity to contribute to the development of an autonomous robot soccer table. There is flexibility in the project for the participant to choose an aspect of the research that is of most interest to them. The hardware is substantially complete but there is scope to experiment and improve upon it. The existing software uses a modular structure with separate modules for image processing, artificial intelligence, and position control. Different modules can be developed so that different approaches can be tried and compared. At present, only very simple modules have been written to test the hardware. The project will involve writing new, more advanced modules. For example, the participant may choose to build an AI for the robot using a deep-learning machine intelligence approach, or by using a rule-based approach based on a cognitive architecture.
Supervisor: Dr Braden Phillips

Classifying Network Traffic Flows with Deep-Learning
Description: Deep-learning or Deep Neural Networks has gained prominence in recent years in a range of application areas, including image classification, speech recognition, self-driving cars, and was successfully adopted by IBM and Google for their artificial intelligence projects in winning competitions such as Chess and Go. This project involves developing deep learning techniques for classifying internet communications traffic for monitoring and management of networks and their infrastructure. Malicious attacks against computer networks of businesses, government agencies and the wider Internet infrastructure is another critical area of concern due to their increasing frequency and resultant damage.

This project expands upon current network classification R&D projects sponsored by the Defence Science & Technology Group since 2014. The goal of this project is to extend existing research and techniques for classification of sparsely labelled network data. In discussion with the successful student(s), this includes expanding the deep-learning approach with graph theoretic methods, self-taught or transfer-learning concepts.
The project provides students with the opportunity to:

- Gain knowledge within the data sciences domain, specifically deep-learning technologies
- Develop and adapt machine-learning techniques for application to network traffic flows
- Gain experience in utilising the university's super computing platform (HPC) to deploy traffic classifiers and conduct experiments
- Collaborate and write a research paper to capture the research work undertaken

Supervisors: Dr Hong-Gunn Chew and Dr Adriel Cheng

Efficient Implementation of Neural Networks in Hardware
Description: Deep learning neural networks have recently brought about major advances in areas such as automatic speech recognition, image recognition, natural language processing, and user recommendation systems. While neural networks are usually implemented on CPUs and/or GPUs, either singly or in clusters, neural networks have also previously been implemented in both FPGAs and proprietary ASICs. In almost all implementations, the most expensive processes for a neural network (in terms of speed, power usage, and physical size in hardware implementations) are the calculations of the neural activation function from weighted-sums of the neurons input. This project will explore a novel, efficient implementation of neural networks in hardware that minimises the expense of the neural activation function calculations while retaining the applicability of training the neural network to general test cases.
Supervisor: Dr Braden Phillips